REMARKS

The claims have been amended in view of the Office action and in view of the remarks which follow, they are believed to be in condition for allowance. The specification has been amended to clarify and elucidate written description of features shown in the drawings.

Epitaxial Raised Source/Drain Regions and the Problem of Formation of Unwanted Spurious Epitaxial Silicon Nodules

The specification, abstract and claims have been amended to explain the problem of formation of unwanted spurious epitaxial, silicon nodules on the top edges of the gate electrode during formation of epitaxial Raised Source/Drain (RSD) regions 28S/28D in cases in which the protective sidewall spacers on the sidewalls of the gate electrodes have left a portion of the upper sidewalls of the gate electrode exposed prior to the epitaxial deposition of silicon on the top surface of the semiconductor substrate to form the RSD regions 28S/28D. In that case, in the prior art the exposed surface of the polysilicon of the gate electrode has received unwanted deposits of epitaxial silicon forming spurious silicon nodules 28T on the tops of the gate electrode sidewalls simultaneously with the formation of the epitaxial RSD regions 28S/28D on the top surface of the thin silicon semiconductor layer 12. The problem that needed to be solved was to form RSD regions in FET devices in which spurious silicon nodules have been prevented from forming in on the top sidewalls of the gate electrodes. While that point was not explained as clearly as it is above, there is adequate description of those facts as explained next, below.

Paragraph [0022] of the published version of the instant application reads as follows:

> "FIGS. 2A and 2B are analogous to FIGS. 1A and 1B, showing the structure before and after the formation epitaxial raised source/drain regions 28S/28D."

Paragraph [0005] of the published version of the instant application reads as follows:

> "FIG. 1B shows the device 10 of FIG. 1A after growth of the raised source 28S and the raised drain 28D on the surface of the thin silicon layer 12. T he problem which is illustrated by FIG. 1B is that the exposure of the upper corners of the gate electrode 18 has led to spurious growth of silicon nodules 28T is seen in the region exposed at the top corners of the gate electrode 18."

Paragraph [0006] of the published version of the instant application reads as follows:

"The process requirement in the past has been to protect the polysilicon of the gate polysilicon 18 with spacers 16 for the purpose of avoiding the formation of spurious epitaxial growth during the raised source drain formation."

[Paragraph [0008] of the published version of the instant application reads as follows:

"The process of formation of raised source/drain regions suffers from a very limited process window. Any exposure of the gate polysilicon through either the hard mask 22 and/or above the sidewall spacers 16 results in unwanted epitaxial growth of silicon nodules 28T on the upper surfaces of the gate electrode 18 where they are exposed."

It is respectfully submitted that the above paragraphs clearly explain the problem which is caused by the unwanted formation of "spurious epitaxial growth" of silicon nodules 28T on the upper corners of the of the gate electrode 18. The amendments to the specification and the claims make this point crystal clear.

Claim Rejections - 35 U.S.C. § 103

In section 3 of the Detailed Action, under 35 U.S.C. 103 (a), claims 29-39 were rejected as being unpatentable over Gilton (US Pat. 6,143,611) in view of Chang et al. (US Pat, 6,030,863, herein after Chang).

With respect to Gilton, the Office Action stated as follows:

"Gilton discloses in figs. 5- 7 an SOI MOSFET device (col. 1, lines 24-28) comprising:
a substrate 32 with a top substrate surface upon which a gate electrode stack is formed;
gate electrode stack (col. 3, line 62 through col. 4, line 1) comprising:
a polysilicon gate electrode 34 formed over a gate dielectric layer 33,
gate dielectric layer 33 being formed on top substrate surface 32;
polysilicon gate electrode 34 having a top gate electrode surface and having gate electrode sidewalls; sidewall spacers 50 formed on gate electrode sidewalls aside from gate electrode 34;
a cap layer 35 having outer edges and a top formed on top gate electrode surface;
a hard mask 39 formed on top of cap 35; notches formed in outer edges of cap layer 35 recessed from gate electrode sidewalls;
notches in outer edges of cap layer 35 being filled with protective plugs 50 formed on top of gate electrode layer 34 (col. 5, lines 11-33); and
sidewall spacers 50 reaching along polysilicon gate electrode sidewalls to above a level at which protective plugs 50 contact gate electrode 34 whereby sidewall spacers 50 are contiguous with and overlapping protective plugs 50 covering sidewalls of polysilicon gate electrode 33 and a raised source/drain region 62/64 on top of said silicon layer 32 aside from spacers 62 (col. 5, lines 42-47)."
"Gilton discloses the gate electrode comprising a polysilicon gate electrode 34 and a cap layer 35 having a notches formed in outer edges of cap layer 35 recess [sic] from gate electrodes sidewalls but fails to disclose the cap layer is an implanted amorphous silicon layer formed of germanium and silicon ions. However, Chang teaches amorphous silicon/amorphous silicon-germanium 60/polysilicon layer 20 is used for the gate electrode material (fig. 4 and col. 5, lines 12-

20). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Gilton by using the gate electrode material as taught by Chang, in order to increase the conductivity of the gate electrode (See Abstract). Noted that the process of forming polysilicon/amorphous cap layer of Chang (fig. 4 and col. 5, lines 12-20) and that of the claimed invention is very much the same (see Specification [0028])."

THE PRIOR ART REFERENCES, WHEN COMBINED DO NOT TEACH OR SUGGEST ALL OF THE CLAIM LIMITATIONS AS REQUIRED BY MPEP § 2142

It is respectfully submitted that there is an error in the above ground of rejection in that it refers to "a raised source/drain region 62/64 on top of said silicon layer 32 aside from spacers 62 (col. 5, lines 42-47)."

Gilton Fails to Teach RSD Regions 62 or 64 Atop the Top Surface of Silicon Substrate 32 and Chang Also Fails to Teach RSD Regions

The actual language found at Col. 5, lines 41-46 of Gilton reads as follows:

> "Referring to FIG. 7, insulative material is formed over oxide layer 50 and is subsequently anisotropically etched to produce insulative illustrated spacers 62. Subsequent ion implanting can then be conducted to provide dopant impurity into substrate 32 proximate the gate stack to form field effect transistor source/drain regions 64.

It is respectfully submitted that it is manifest that the Office Action made an incorrect allegation concerning RSD regions. First, there are no *source/drain regions 62 in Gilton. Reference number 62 refers to spacers, not source/drain regions.* There are buried (not raised) *source drain/ regions 64* which are manifestly located in the silicon substrate 32, as is plainly shown by FIG. 7 where they were formed by ion implantation into the silicon substrate 32, not by epitaxial deposition on top of the top surface of the substrate 32. Accordingly, it is respectfully requested that the allegation that Gilton teaches an RSD structure should be withdrawn.

Second please note that substrate 32 is a substrate, not a "layer" as alleged in the Office Action. Substrate 12 is described as "a bulk monocrystalline substrate 12" at Col. 2, lines 28-31 of Gilton, not as a silicon layer. On the other hand, in Gilton the "silicon layer" comprises the gate electrode layer referred to at Col. 3, lines 62-65 of Gilton as "conductively doped silicon layer 34 (i.e., polysilicon)" which layer 34 was employed to form a portion of the "conductive gate stack 38" in FIG. 4 (Col. 4, lines 6-10 of Gilton).

The claims have been amended so that all of the claims recite "a raised source region and a raised drain region formed on top of said top substrate surface of said substrate aside from said sidewall spacer material" which is not shown by Gilton, even when it is combined with Chang et al. As indicated above MPEP § 2142 states "Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations." Accordingly, it is respectfully submitted that in view of the amendments to the claims the grounds of rejection are now believed to be moot and should be withdrawn since the source/drain regions in both references are contained within the substrate, below the top surface thereof, not on top of the top surface thereof. Moreover, Chang does not relate to MOSFET devices formed on SOI substrates and Gilton does not show an SOI substrate but merely defines a semiconductor substrate as including SOI substrates in the Background of the Invention thereof.

NO SUGGESTION OR MOTIVATION, EITHER IN THE REFERENCES THEMSELVES OR IN THE KNOWLEDGE GENERALLY AVAILABLE TO ONE OF ORDINARY SKILL IN THE ART, IS FOUND TO MODIFY THE REFERENCE OR TO COMBINE REFERENCE TEACHINGS

In chapter 2100 entitled Patentablilty in a MPEP § 2142 provides under "ESTABLISHING A *PRIMA FACIE* CASE OF OBVIOUSNESS" reads as follows:

"To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). See MPEP § 2143 - § 2143.03 for decisions pertinent to each of these criteria."

"2143.01 Suggestion or Motivation to Modify the References [R-3]"

"I. THE PRIOR ART MUST SUGGEST THE DESIRABILITY OF THE CLAIMED INVENTION"

"There are three possible sources for a motivation to combine references: the nature of the problem to be solved, the teachings of the prior art, and the knowledge of persons of ordinary skill in the art.' *In re Rouffet*, 149 F.3d 1350, 1357, 47 USPQ2d 1453, 1457-58 (Fed. Cir. 1998) (The combination of the references taught every element of the claimed invention, however without a motivation to combine, a rejection based on a *prima facie* case of obvious was held improper.). The level of skill in the art cannot be relied upon to provide the suggestion

to combine references. *Al-Site Corp. v. VSI Int'l Inc.*, 174 F.3d 1308, 50 USPQ2d 1161 (Fed. Cir. 1999).

"In determining the propriety of the Patent Office case for obviousness in the first instance, it is necessary to ascertain whether or not the reference teachings would appear to be sufficient for one of ordinary skill in the relevant art having the reference before him to make the proposed substitution, combination, or other modification.' *In re Linter*, 458 F.2d 1013, 1016, 173 USPQ 560, 562 (CCPA 1972)."

"Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. 'The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art.' *In re Kotzab*, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). See also *In re Lee*, 277 F.3d 1338, 1342-44, 61 USPQ2d 1430, 1433-34 (Fed. Cir. 2002) (discussing the importance of relying on objective evidence and making specific factual findings with respect to the motivation to combine references); *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

Applicants submit that the problem of formation of "silicon nodules" on the top edge of the polysilicon of the gate electrode is not suggested by either of the references as required by section MPEP 2143.01. In the in paragraph [0005] of the publication of the present application, it is stated as follows:

> "The problem which is illustrated by FIG.1B is that the exposure of the upper corners of the gate electrode 18 has led to spurious growth of silicon nodules 28T is seen in the region exposed at the top corners of the gate electrode 18."

The problem dealt with by Gilton is not formation of epitaxial or other silicon nodules or deposits on the top of the gate electrode, but it is short-channel effects which are reduced by reducing gate-to-drain overlap capacitance, as stated at Col. 1, lines 38-58 of Gilton as follows:

> "Integrated circuitry fabrication technology continues to strive to increase circuit density, and thereby minimize the size and channel lengths of field effect transistors. Improvements in technology have resulted in reduction of field effect transistor size from long-channel devices (i.e., channel lengths greater than two microns), to short-channel devices (i.e., channel lengths less than two microns), and to sub-micron devices (i.e., channel lengths less than one micron). As field effect transistor channel lengths (i.e., gate or word line widths) became smaller than two microns, so-called short-channel effects began to become increasingly significant. As a result, device design and consequently process technology had to be modified to take these effects into account so that optimum device performance could continue to be obtained. For example, the lateral electrical field in the channel region increases as a result of smaller transistor

channel lengths as the supply voltage remains constant. If the field becomes strong enough, it can give rise to so-called hot-carrier effects. Hot-carrier effects often lead to gate oxide degradation, as energetic carriers can be injected into gate oxide and become permanent charges."

"Two recognized solutions to this problem, used either alone or in combination, include source/drain re-oxidation and provision of lightly doped drain (LDD) regions. Source/drain re-oxidation effectively grows a layer of thermal oxide over the source and drain areas as well as over the gate sidewalls. The oxidation has the effect of rounding the poly gate edge corners in effectively oxidizing a portion of the gate and underlying substrate, thereby increasing the thickness of the gate oxide layer at least at the edges of the gate. Such reduces the gate-to-drain overlap capacitance, and strengthens the gate oxide of the polysilicon gate edge. The latter benefits are effectively obtained because oxidation-induced encroachment gives rise to a graded gate oxide under the polysilicon edge. The thicker oxide at the gate edge relieves the electric-field intensity at the corner of the gate structure, thus reducing short-channel effects."

It is respectfully submitted that the grounds of rejection stated under 35 U.S.C. § 103 are believed to be moot in view of amendments to the claims for the reasons stated above and below.

Gilton Teaches Formation of a Refractory Metal Silicide Layer as a Cap Layer Above a Gate Polysilicon Layer but Gilton Does Not Teach a Cap Comprising a Notched Amorphous Layer Formed in the Surface of a Gate Polysilicon Structure with the Notch Filled with a Plug

It is respectfully submitted that it is believed to be very clear that the refractory metal silicide cap layer 35 of Gilton is very different from the amorphous silicon cap layer 21 of the instant invention since the amorphous silicon cap layer 21 of the instant invention is an amorphous layer formed in the top surface of the gate polysilicon whereas the cap layer 35 of Gilton comprises a separate refractory metal silicide (e.g. (WSi_x)) layer formed above the gate polysilicon layer 34.

Thus a significant distinction from Gilton is that there is no amorphous silicon layer formed on top of the silicon (polysilicon) layer 34. Moreover, Gilton has no notch in an amorphous layer as taught and claimed herein. Instead, in Gilton there is an unnumbered recess (shown at the end of arrow from indicia 38 in FIG. 5) which is formed in the refractory metal silicide layer 35, but not in an amorphous silicon layer. That is an entirely different structure from what is claimed by the amended claims of the instant application.

Chang Does not Suggest or Teach the Solution to the Problem of Silicon Nodules Formed on the Sidewalls of the Gate Polysilicon of a Gate Electrode by a Provision of a Notch Formed in an Amorphous Layer of the Gate Polysilicon

It is respectfully submitted that the present invention is directed to provide a structure which does not have the problems of spurious growth structures formed on exposed portions of the sidewalls of polysilicon gate electrodes. It is respectfully submitted that the teachings of Gilton have no relationship to the problem of spurious growth structures formed upon exposed portions of the sidewalls of polysilicon gate electrodes. Moreover, the problem and the solution are neither addressed nor is a structure which provides a solution to that problem suggested by the Gilton reference.

Attention is called to the fact that the rejection included the phrase *"in order to increase the conductivity"* with reference to Chang In the context of the present invention which relates to a notch formed in the amorphous surface of a gate electrode structure to prevent growth of silicon nodules, the problem of *conductivity* addressed by Chang is respectfully submitted to be clearly irrelevant to the problem of providing a product without spurious silicon nodules formed on the tops of the gate electrode structure. The present invention is focused upon elimination of the presence of such spurious silicon nodules, *but has nothing to do with "increasing conductivity"* which is not mentioned anywhere in the present application. In other words, the problem of spurious nodules at the top of the polysilicon of a gate electrode which is solved by the structures defined by the claims pending herein and which is discussed in detail in the present application and hereinabove is not in any way related to the problem addressed by Chang.

It is respectfully submitted that the teaching of Chang of implanting of germanium into the surface of the gate structure to form amorphous layer 60 is performed after the formation of the sidewall spacers 50 without any conception of notches in the gate electrode stack filled with a plug. It is believed to be manifest that Chang does not suggest the presence of notches or recesses in the edges of the amorphous layer 60, so the structure is substantially different and the problem addressed is also entirely different.

In particular, the amendments make it clear that of the gate polysilicon of the gate electrode stack includes an amorphous silicon layer formed in the top gate electrode surface which

has notches formed in outer edges thereof. There is no showing in either Gilton or Chang of notches in an amorphous silicon layer in the gate polysilicon of a gate electrode stack. Clearly the layer 35 of Gilton comprises a silicide layer (e.g. tungsten silicide (WSi_x)), not a cap layer composed of amorphous silicon. Accordingly, in view of that significant distinction it is respectfully submitted that the amended claims are not suggested by the combination of Gilton and Chang. Moreover, while Chang teaches an amorphous region 60 implanted into the surface of a gate polysilicon structure, it fails to suggest the concept of forming a notch in the edge of an amorphous silicon cap layer filled with a protective plug. Thus in addition that neither reference relates to FET devices with RSD regions, neither reference suggests formation of a notch in an amorphous silicon cap layer in the gate polysilicon.

In particular, Chang teaches formation of an amorphized layer 60 in the surface of the polysilicon gate 20 after formation of the extension layers 24/44, *i.e. after, not before*, formation of sidewall spacers 22. At Col. 4, lines 42-67 Chang reads as follows:

> "An ion implant is next performed to form the lightly doped drain regions 24 and 44. The gate electrodes 20, 40 serve as a mask, shielding the gate regions 18 from the implant, thereby making the source and drain regions self-aligned to the gate. Using a block out mask, the PMOS device 6 is covered while the source and drain regions 44 of the NMOS device 8 is implanted with an n-type dopant, for example arsenic or phosphorous. Similarly the NMOS device 8 is masked while the source and drain regions 24 of the PMOS device 6 are implanted with a p-type dopant, typically boron."

> "By depositing a conformal layer of silicon oxide over the wafer and anisotropically etching this layer back to the silicon by RIE, the sidewall spacers 22 are formed alongside the gate electrodes 20 and 40. Alternately, the sidewall spacers 22 may be formed of other suitable materials such as silicon nitride. Next, using a block out mask method, the heavily doped source and drain regions 26 and 46 are implanted using arsenic or phosphorous for the NMOS 8 device and boron for the PMOS device 6. The source/drain implants of the NMOS device 8 are formed using arsenic at a dose of $4x10^{15}$ atoms cm^{-2} or thereabout at an energy of 30 keV or thereabout. The source/drain implants of the PMOS device 6 are formed using BF_2^+ at a dose of $5x10^{15}$ atoms cm^{-2} or thereabout at an energy of 20 keV or thereabout."

Referring to Chang at Col. 5, lines 11-27, it is stated as follows:

> "Referring now to FIG. 4, the wafer is blanket implanted with germanium. A conventional ion implanter, such as the model 9500 xR manufacture by Applied Materials Corp., of Santa Clara Calif., may be used. The germanium is implanted at a dose of between about $3x10^{14}$ and $2x10^{15}$ atoms/cm^2 at a energy of between about 20 and 60 keV.

The implantation forms a region 50 on the surface of the source/drain region 26 which is amorphized to a depth of about 300 to 800 Å. A corresponding region 60 on the polysilicon gate 20 is similarly amorphized to a depth of about 300 to 800 Å."

"Next, the wafer is blanket implanted with arsenic at an energy of between about 5 and 10 keV at a dose of between about $5x10^{13}$ and $5x10^{14}$ atoms cm^{-3}. his energy places the centroid of the low dosage implant in a region 52 less than about 100 Angstroms beneath the silicon surface with a straggle of less than about 30 Angstroms. A corresponding arsenic implanted region 62 is formed on the polysilicon gate 40."

In summary, the claims have been amended to make it clear that the notch is formed in the "amorphous polysilicon of the gate electrode," so it is believed that the rejection if now moot. In Gilton there is an insulating layer 36 (i.e., doped or undoped SiO_2, Si_3N_4, etc.) are formed over monocrystalline substrate 32 silicide layer 35. Neither Gilton nor Chang et al teaches (1) Raised Source/Drain Regions 64 and (2) a notch in an amorphous layer filled with a plug.

In paragraphs 0006 and 0008 of the published version of the instant application, the problem of spurious growth of silicon nodules is described as being caused by exposure of the top of the gate polysilicon by "spacer pull down" and in paragraphs 0009 and 0010 applicants stated that the object of the present invention is to prevent this exposure. Spacer pull down is discussed in paragraph [0023] of the instant application which reads as follows:

"[0023] FIG. 2A shows spacer pull down to the same level as FIG. 1A, but the dielectric plug 26P prevents exposure of the polysilicon of the gate electrode 18 during the step of forming the raised source/drain regions 28S/28D."

The original abstract of the present application stated as follows:

"A method is provided for forming an SOI MOSFET device with a silicon layer formed on a dielectric layer with a gate electrode stack, with sidewall spacers on sidewalls of the gate electrode stack and raised source/drain regions formed on the surface of the silicon layer. The gate electrode stack comprises a gate electrode formed of polysilicon over a gate dielectric layer formed on the surface of the silicon layer. A plug of dielectric material is formed in a notch in a cap layer above the gate polysilicon. The sidewalls of the gate electrode is covered by the sidewall spacers which cover a portion of the plug for the purpose of eliminating the exposure of the gate polysilicon so that formation of spurious epitaxial growth during the formation of raised source/drain regions is avoided."

Paragraph [0024] of the instant application reads as follows:

"[0024] FIG. 2B shows the device 10 of FIG. 2A after formation of the raised source/drain regions 28S/28D with the improvement that the epitaxial growth is only at the site of the source region 28S and drain regions 28D. There is no spurious growth on the top corner of the polysilicon of the gate electrode 18 of the kind seen in FIG. 1B."

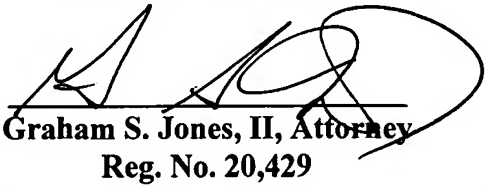
It is believed that the above paragraphs from the original application manifest the difference between the structure claimed herein and the distinctions from the prior art of record.

In summary, it respectfully submitted that the prior art references fail to teach the subject matter of the amended claims even when combined because they do not relate to RSD (Raised Source/Drain) devices, and neither relates to the problem of providing RSD FET devices with no epitaxial spurious nodules on the top corners of the gate electrodes. Finally, it respectfully submitted that there is nothing in the prior art cited which would motivate one to combine the teachings of Gilton with the teachings of Chang.

If additional fees are required, please charge such fees to Deposit Account No. 09-0458.

In view of the amendments and the above remarks favorable action including allowance of the claims and the application as a whole are respectfully solicited.

Respectfully submitted,



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